COURSE DESCRIPTION CARD - SYLLABUS

Course name
Digital systems design [S1EiT1E>TC]

Course

Field of study
Electronics and Telecommunications

Year/Semester
2/3

Area of study (specialization)
–

Profile of study
general academic

Level of study
first-cycle

Course offered in
English

Form of study
full-time

Requirements
compulsory

Number of hours

Lecture
30

Laboratory classes
0

Other (e.g. online)
0

Tutorials
30

Projects/seminars
0

Number of credit points

4,00

Coordinators

dr hab. inż. Maciej Krasicki
maciej.krasicki@put.poznan.pl

Lecturers

Prerequisites

Fundamentals of algebra, and computer science, an ability to analyze and design simple electrical circuits and devices, ability to acquire knowledge from the technical literature in English.

Course objective

The course aim is to provide students with the principles of digital circuit design, including both theoretical paradigms and a practical guide. The presentation starts from Boolean algebra principles and then moves on synthesis of both combinational logic and finite state machines. At the right time, several integrated circuits, like multiplexers, arithmetic logic units, registers, counters, etc., are introduced. Afterwards, hardware description languages along with their application for VLSI devices are demonstrated. The presentation finishes with a glimpse into circuit fault issues. Throughout the course students are exposed to modern technologies, and are motivated to develop their logical thinking skills by designing digital circuits in an effective way.

Course-related learning outcomes

Knowledge:
1. A student knows how to describe the function of logic circuits, understands various data

representation, and knows how to implement arithmetic operations on hardware, including both fixed and floating-point addition, subtraction, multiplication and division.
2. A student knows several building blocks (like multiplexers, demultiplexers, registers, counters, arithmetic-logic unit) used in digital circuits design; he/she is familiar with complex digital systems, such as one- and two-dimensional combinational iterative devices and finite state machines (synchronous and asynchronous) working in accordance with the Mealy and Moore paradigms.
3. A student has a preliminary knowledge regarding fault sources and detection procedure in digital VLSI designs and is familiar with the methods used to design reliable and easy to test digital circuits and systems.

Skills:
1. A student can minimize a combinational digital circuit, represented either as a two-level Boolean expression or a multi-level and multi-output circuit in order to reduce hardware complexity, its power consumption, and latency.
2. A student can design and assemble both synchronous and asynchronous finite state machines (including state minimization, state coding, flip-flop-based implementation, and safety analysis).
3. A student can use fault models and find proper test vectors to detect given faults.

Social competences:
A student appreciates the practical significance of the systems developed in the course.

Methods for verifying learning outcomes and assessment criteria

Learning outcomes presented above are verified as follows:

Learning outcomes presented above are verified as follows:
In semester III, there are two tests (in the middle, and at the end of the semester). Each test is worth 1/3 of the total amount of base points that can be earned for the tutorials. Remaining 1/3 of base points can be obtained from short entrance tests, organized ad-hoc. A student must reach half of the base points to pass and obtain a positive grade from tutorials. The students get extra credits for their volunteering to solve tasks at the blackboard. They could increase the final grade unless they fail to cross the threshold for the base points.
In semester IV, the students obtain their credits for developing solutions to problems considered during the lab classes, so their progress is evaluated during the course, and the mark for lab classes bases on it. Students can also expect some short entrance tests verifying their knowledge. The points impact on the final lab class grade.
The exam is planned for semester IV. It is a written test, which covers selected topics presented during the lecture. The students get some problems to solve according to their knowledge.

Programme content

Boolean algebra, design of combinational and sequential circuits

Course topics

Lecture - semester III: overview of numeral systems (positional systems, complement arithmetic, signed numerals, protective codes, BCD codes, floating point number representation), Boolean algebra (postulates, laws, functionally-complete system, logic gates, cannonical forms of logic expressions, logic minimization, Karnaugh maps), combinational blocks (MSI chips, decomposition, multiplexers, demultiplexers), arithmetic logic (Ripple-Carry Adder, Carry Look-Ahead Adder, CLA chip, Carry Save Adder, Carry-Select Adder, Arithmetic Logic Unit, C2 subtraction, matrix multiplication, serial add-shift multiplication, BCD adder), basic sequential circuits (RS latch, master-slave latch, flip-flops: D, T, JK, registers, ring counter, Johnson"s counter, ripple counter, synchronous decade counter, linear-feedback shift register)
Tutorials - semester III: numeral systems (converting system base, signed and unsigned formats, BCD, floating point arithmetic), Boolean algebra (use of algebraic laws and postulates to simplify Boolean expressions, full cannonical form, Karnaugh-map minimization), design of combinational circuits (with logic gates, only, or with multiplexers/demultiplexers)
Lecture - semester IV: design of synchronous automata (Moore- and Mealy-convention, state diagrams, automaton minimization, state coding, hardware assembly), asynchronous automata (anti-race coding, automaton minimization), Register Transfer Level design (datapath and control unit, algorithmic state

machine chart), programmable logic devices (PLA, FPGA, CPLD, PicoZed example), hardware description languages, testing of digital circuits (sensitized path method, D-algebra, testing strategies, undetectible faults, testing of sequential digital circuits, testability, built-in self tests, test compacting)
Lab classes - semester IV: tutorial guide to MultiSim, NAND-NAND combinational circuit, MUX/DEMUX-based circuit, iterative combinational circuit, sequencer (with general-purpose flip-flops or integrated decade counter or LFSR), synchronous and asynchronous automaton design

Teaching methods

Lecture: slide presentation with extra comments and practical examples solved on the blackboard.
Tutorials: the students each time get a set of tasks printed on paper; the students works in groups to develop the solution, then volunteers or people selected by the teacher solve the task at the blackboard. Some of the tasks are the students" homework.
Lab classes: The students design logic circuits using MultiSim software, according to the teacher"s instruction.

Bibliography

Basic:
M. Morris Mano, Digital Design: With an Introduction to the Verilog HDL, Ed. 5, Pearson, 2011 (PDF available)
V. Nelson, Digital logic circuit analysis and design, Prentice-Hall, 1995
P. Remlein, Digital Systems Design - Exercises, student guidebook, 2015 (distributed by the teacher)
Additional:
J. Wakerly, Digital design - principles and practices, Ed. 4, Prentice-Hall, 1999 (PDF available)

Breakdown of average student's workload

	Hours	ECTS
Total workload	200	8,00
Classes requiring direct contact with the teacher	125	5,00
Student's own work (literature studies, preparation for laboratory classes/ tutorials, preparation for tests/exam, project preparation)	75	3,00